

Course Description

Use the ISE™ software tools to implement a design and gain a firm understanding of the Xilinx FPGA architecture. Learn the best design practices from the pros and understand the subtleties of the Xilinx design flow.

This course covers ISE 8.2i features, such as the Architecture Wizard and the Pin and Area Constraint Editor (PACE). Other topics include design planning, implementation options, and global timing constraints. For more emphasis on improving the overall design performance, take the follow-up course *Designing for Performance*, which builds on the basic principles covered in this course.

Level – Fundamental

Course Duration – 1 day

Price – \$500 USD or 5 Training Credits

Course Part Number – FPGA13000-8.2-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- Basic FPGA Architecture: Slice and I/O Resources REL*
- Basic FPGA Architecture: Memory and Clocking REL*
- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Software Tools

- Xilinx ISE 8.2i

After completing this comprehensive training, you will have the necessary skills to:

- Use Xilinx Project Navigator to implement an FPGA design
- Assign pin locations with the PACE tool
- Create DCM instantiations with the Architecture Wizard
- Read reports to determine whether design goals were met
- Use the Constraints Editor to enter basic global timing constraints
- Locate and modify implementation options

Course Outline

- Course Agenda
- Review of Basic FPGA Architecture
- Xilinx Tool Flow
- **Lab 1:** Xilinx Tool Flow Lab
- Reading Reports
- Architecture Wizard and PACE
- **Lab 2:** Architecture Wizard and PACE Lab
- Global Timing Constraints
- **Lab 3:** Global Timing Constraints Lab
- Implementation Options
- **Lab 4:** Implementation Options Lab
- Synchronous Design Techniques
- Course Summary

Lab Descriptions

- **Lab 1:** Xilinx Tool Flow – Create a new project in the ISE Project Navigator and use the Architecture Wizard and PACE tool in the design process. Implement a design by using default software options. The design will be simulated.
- **Lab 2:** Architecture Wizard and PACE – Use the Architecture Wizard to customize a DCM and incorporate the DCM into the design. Use PACE to assign pin locations and implement the design.
- **Lab 3:** Global Timing Constraints – Enter global timing constraints with the Xilinx Constraints Editor. Review the Post-Map Static Timing Report to verify that the timing constraints are realistic. Use the Post-Place & Route Static Timing Report to determine the delay of the longest constrained path for each timing constraint.
- **Lab 4:** Implementation Options – Adjust process properties and I/O configuration options to improve the design performance.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

* Recorded e-Learning