

## Course Description

Learn how signal integrity techniques are applicable to high-speed interfaces between Xilinx FPGAs and semiconductor memories. This course teaches you about high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using CAD packages. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules and practical hands-on labs.

**Level** – Intermediate

**Course Duration** – 2 days

**Price** – \$1000 USD or 10 training credits

**Course Part Number** – SI20000-6-ILT

**Who Should Attend?** – Digital designers, board layout designers, or scientists, engineers, and technologists seeking to implement Xilinx solutions. Also end users of Xilinx products who want to understand how to implement high-speed interfaces without incurring the signal integrity problems related to timing, crosstalk, and overshoot or undershoot infractions.

**Prerequisites**

- Xilinx FPGA design experience preferred (equivalent of *Fundamentals of FPGA Design* course)

**Software Tools**

- Mentor Graphics HyperLynx<sup>®</sup>
- Cadence SPECCTRAQuest<sup>®</sup>

After completing this comprehensive training, you will have the necessary skills to:

- Identify when signal integrity is important and relevant
- Interpret an IBIS model and correct common errors
- Apply appropriate transmission line termination
- Understand the effect loading has on signal propagation
- Mitigate the impact of jitter
- Manage a memory data bus
- Understand the impact of selecting a PCB stackup
- Differentiate between on-chip termination and discrete termination

## Course Outline

### Day 1

- Introduction
- Transmission Lines
- **Mentor or Cadence Lab 1**
- IBIS Models
- **Mentor or Cadence Lab 2**
- **Mentor or Cadence Lab 3**
- High-Speed Clock Design
- **Mentor or Cadence Lab 4**
- SRAM Requirements
- **Mentor or Cadence Lab 5**

### Day 2

- Physical PCB Structure
- On-Chip Termination
- SDRAM Design
- **Mentor Lab 6**
- Managing an Entire Design

### Lab Descriptions

**Note:** Labs feature the Mentor Graphics or Cadence flow. For private training, please specify your flow to your registrar or sales contact. For public classes, flow will be determined by the instructor based upon class feedback.

- **Mentor Lab 1:** Opening the appropriate Mentor simulator
- **Mentor Lab 2:** Hands-on signal integrity observation of reflection and propagation effects
- **Mentor Lab 3:** Using an IBIS simulator to study basic transmission line effects
- **Mentor Lab 4:** Using saved simulation information to perform power calculation. Also, additional clock simulations
- **Mentor Lab 5:** Observing the effects of coupling on transmission lines
- **Mentor Lab 6:** Demonstrating how an SDRAM module can be handled with an EBD model
- **Cadence Lab 1:** Opening the appropriate Cadence simulator
- **Cadence Lab 2:** Analysis of a simple clock net
- **Cadence Lab 3:** Signal integrity effects caused by multidrop clock networks
- **Cadence Lab 4:** Crosstalk analysis
- **Cadence Lab 5:** Address and data analysis

## Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.