

Course Description

This comprehensive course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization. This course covers Verilog 1995 and 2001.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Level – Fundamental to Intermediate

Course Duration – 3 days

Price – \$1500 USD or 15 Training Credits

Practical HDL Multimedia CD – \$300 USD or 3 Training Credits

Course Part Number – LANG12000-8-ILT

Who Should Attend? – Engineers who want to use Verilog effectively for modeling, design, and synthesis of digital designs

Prerequisites

- Basic digital design knowledge

Software Tools

- ISE™ 8.1i
- Xilinx ISIM Simulator
- Synplicity Synplify Pro
- Synopsys SmartModels

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Run a timing simulation by using Xilinx Simprim libraries
- Create and manage designs by using the ISE software design environment
- Implement Verilog 2001 language enhancements

Course Outline

Day 1

- Hardware Modeling Overview
- Verilog Language Concepts
- Memories, Modules, and Ports
- **Lab 1:** Building Hierarchy
- Introduction to Testbenches
- **Lab 2:** Verilog Simulation and RTL Verification
- Operators and Expressions

Day 2

- Data Flow-Level Modeling
- **Lab 3:** Memory

- Verilog Procedural Statements
- Controlled Operation Statements
- **Lab 4:** n-bit Binary Counter and RTL Verification
- Advanced Language Concepts
- **Lab 5:** Comparator

Day 3

- Tasks and Functions
- **Lab 6:** Arithmetic Logic Unit
- Finite State Machines
- **Lab 7:** Finite State Machine
- Targeting Xilinx FPGAs
- **Lab 8:** Calculator

Lab Description

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

Register Today

Technically Speaking, Inc is the Xilinx ATP (Authorized Training Provider) for the North American Southwest region, including: southern California, Arizona, New Mexico and Nevada. TSI also delivers public and customized private courses in locations throughout the world.



To register for any course, or to discuss customized onsite training, contact TSI at **(702) 736-4116** or toll free at **(800) 706-4HDL**. Or register for public courses online at www.technicallyspeaking.com/register.htm

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

Practical HDL is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

Cost - \$300 USD

