

## Course Description

This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall VHDL proficiency and prepare you for the *Advanced VHDL* course.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no VHDL knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

**Level** – Fundamental to Intermediate

**Course Duration** – 3 days

**Price** – \$1500 USD or 15 Training Credits

**Practical HDL** Multimedia CD – \$300 USD or 3 Training Credits

**Course Part Number** – LANG11000-8-ILT

**Who Should Attend?** – Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs

**Prerequisites**

- Basic digital design knowledge

**Software Tools**

- ISE™ 8.1i
- Xilinx ISIM Simulator
- Synplicity Synplify Pro
- Synopsys SmartModels

After completing this comprehensive training, you will have the necessary skills to:

- Use VHDL to build hardware models
- Declare and use signals, variables, arrays, and records
- Use VHDL process statements
- Create synthesizable RTL source code
- Run a behavioral simulation, pre- and post-P&R
- Synthesize (compile to hardware) VHDL using XST
- Run a timing simulation using VITAL libraries
- Write FPGA-optimized code for RAMs, FSMs, etc.
- Synthesize RTL code and implement a design in Xilinx FPGAs
- Create VHDL subprograms, functions, and procedures

## Course Outline

### Day 1

- Course Agenda
- Hardware Modeling Overview
- Language Concepts
- Lab 1:** Building Hierarchy
- Introduction to Testbenches
- Lab 2:** VHDL Simulation and RTL Verification
- Signals and Data Types
- VHDL Operators and Expressions
- Lab 3:** Memory and Record

### Day 2

- Concurrent and Sequential Statements
- Advanced Process Statements
- Lab 4:** n-bit Binary Counter and RTL Verification
- Controlled Operation Statements
- Lab 5:** Comparator
- Behavioral to RTL Coding

### Day 3

- Finite State Machines
- Lab 6:** Arithmetic Logic Unit
- VITAL: VHDL Initiative toward ASIC Libraries
- Lab 7:** State Machines
- Targeting Xilinx FPGAs
- Functions and Procedures
- Lab 8:** Calculator

## Lab Description

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

## Register Today

Technically Speaking, Inc is the Xilinx ATP (Authorized Training Provider) for the North American Southwest region, including: southern California, Arizona, New Mexico and Nevada. TSI also delivers public and customized private courses in locations throughout the world.



To register for any course, or to discuss customized onsite training, contact TSI at **(702) 736-4116** or toll free at **(800) 706-4HDL**. Or register for public courses online at [www.technicallyspeaking.com/register.htm](http://www.technicallyspeaking.com/register.htm)

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

**Practical HDL** is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

**Cost** - \$300 USD

