

Course Description

Learn how to synthesize an algorithm written in MATLAB into a design that is optimized for a Xilinx FPGA. Find out how to make MATLAB coding changes that improve area and performance. Use the floating-to-fixed point and design exploration features of the AccelDSP Synthesis Tool to achieve maximum results. Merge a synthesized MATLAB block into a larger HDL design or System Generator design.

Level – Fundamental

Course Duration – 2 days

Price – \$1000 USD or 10 Training Credits

Course Part Number – DSP12000-8-ILT

Who Should Attend? – Engineers seeking to develop the necessary skills for designing DSP systems using Xilinx AccelDSP software running with MATLAB

Prerequisites

- Fundamentals of MATLAB and the Filter Design Toolbox
- Basics of digital signal processing theory

Software Tools

- Xilinx ISE™ 8.1i SP1
- Xilinx AccelDSP Synthesis Tool 8.1.690
- MATLAB R14 SP3
- Xilinx System Generator 8.1.1
- Mentor Graphics ModelSim® 6.0c PE

After completing this comprehensive training, you will have the necessary skills to:

- Modify a MATLAB script for a DSP algorithm so that it can be synthesized using the AccelDSP Synthesis Tool
- Identify the concepts of quantization as well as specify, monitor, and control bit growth in a MATLAB design
- Modify the MATLAB for a direct form FIR filter into a synthesizable polyphase decimation filter
- Apply coding style changes and AccelDSP directives to optimize a design for performance and efficiency
- Write MATLAB coding changes to add hardware control features to a design
- Merge a synthesized MATLAB block into a larger HDL design
- Export and merge a synthesized MATLAB block into a larger System Generator design

Course Outline

Day 1

- Introduction to AccelDSP Design Flow
- Synthesizable MATLAB
- Quantization
- Multirate Design
- Using AccelWare IP
- Overview of FPGA Architecture

Day 2

- Design Exploration
- Adding Hardware Control
- Coding for Hardware Performance
- Synthesizing Complex Numbers
- Interfacing to System Hardware
- Exporting to System Generator

Lab Descriptions

- **Lab 1: Getting Started** – Learn the basic design flow through the AccelDSP Synthesis Tool.
- **Lab 2: Synthesizable MATLAB** – Modify an unsynthesizable MATLAB design into a design that can be synthesized by AccelDSP.
- **Lab 3: Quantization** – Specify, monitor, and control bit growth in the synthesized design.
- **Lab 4: Multirate Design** – Set up behavioral MATLAB to model the effects of decimation by 2. Create a synthesizable polyphase decimation filter in MATLAB and implement the filter in a Xilinx FPGA.
- **Lab 5: Using AccelWare** – Replace a MATLAB-based polyphase decimation filter with an equivalent Firdecim AccelWare IP block.
- **Lab 6: Design Exploration** – Apply the design exploration features of AccelDSP to optimize a design for area and performance.
- **Lab 7: Adding Hardware Control** – Modify the source MATLAB of a FIR filter to add a serial coefficients load feature.
- **Lab 8: Coding for Hardware Performance** – Learn MATLAB coding techniques to take advantage of even-symmetric coefficients and drive performance over 300 MHz.
- **Lab 9: Synthesizing Complex Numbers** – Explore the methods available for synthesizing designs that use complex numbers.
- **Lab 10: Interfacing to Hardware** – Connect the AccelDSP-generated interface signals to a larger HDL design.
- **Lab 11: Export to System Generator** – Export a MATLAB-based design into a System Generator block and merge the block into a larger System Generator design.

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