

Course Description

Interested in learning how to effectively utilize Virtex™-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed *Fundamentals of FPGA Design* and *Designing for Performance* and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device.

Topics covered include a Virtex-5 FPGA overview, new CLB, DCM and PLL, global and regional clocking techniques, memory, DSP and arithmetic logic, and source-synchronous resources. A combination of modules and labs allow for practical hands-on application of the principles taught.

Note: Recorded e-Learning modules will also be available. For all other regions, only the recorded e-Learning modules will be available. Also note that the initial course material covers the Virtex-5 LX FPGA platform only. Future revisions will include additional platforms as they become available.

Level – Intermediate

Course Duration – 2/3rd of a day (will increase to a full day as the other Virtex-5 FPGA platforms become available)

Price – \$300 USD or 3 Training Credits

Course Part Number – V5LX-23000-8-ILT

Who Should Attend? – For those who have taken the *Fundamentals of FPGA Design* and *Designing for Performance* courses. A comprehensive knowledge of the Virtex-4 family architecture is also required. This material should be considered a Virtex-5 FPGA update course from the Virtex-4 FPGA family.

Prerequisites

- *Fundamentals of FPGA Design* course
- *Designing for Performance* course
- *Designing with the Virtex-4 Family* course or comprehensive knowledge of the Virtex-4 FPGA

Software Tools

- Xilinx ISE™ 8.2i
- Synplicity Synplify Pro 8.6
- Mentor Graphics Precision 2005c

After completing this comprehensive training, you will have the necessary skills to:

- Describe the 6-input LUT of the Virtex-5 FPGA
- Specify the CLB arrangement in the Virtex-5 FPGA
- Define the block RAM resources of the Virtex-5 FPGA
- Differentiate the arithmetic logic resources of the DSP48E slice in the Virtex-5 FPGA
- Identify the clocking resources of the Virtex-5 FPGA

Course Outline

- Virtex-5 FPGA Overview
- CLB Resources
- Clocking Resources
- **Lab 1:** Clocking Resources Lab
- I/O Resources
- Memory Resources
- XtremeDSP Technology Resources
- **Lab 2:** DSP48E Resources Lab

Lab Descriptions

The labs will provide practical hands-on application of the principles taught throughout the course.

Lab 1: Clocking Resources – In this lab, you will create a PLL core by using the Architecture Wizard to generate a PLL core to instantiate in your design. You will then simulate the PLL core to verify functionality.

Lab 2: DSP48E Resources – In this lab, you will create a Multiplexer by using the XtremeDSP™ technology (DSP48E) resource through primitive instantiation. You will then simulate the resources to verify functionality.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and training credits.