

Course Description

Learn to increase design performance and achieve repeatable results by using the PlanAhead™ software tool. Topics include: a product overview, synthesis and project tips, design analysis, creating a floorplan, improving performance, experimenting with implementation options, incremental methodology, and block-based IP design.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead software. This course is supplemented with instructor-led presentations and demos.

Level – Intermediate

Course Duration – 2 days

Price – \$1000 USD or 10 Training Credits

Course Part Number – FPGA11000-8.2-ILT

Who Should Attend? – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

Prerequisites

- *Fundamentals of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE™ software flow
- *Designing for Performance* recommended

Software Tools

- Xilinx ISE 8.2i

After completing this comprehensive training, you will have the necessary skills to:

- Import designs into the PlanAhead software
- Analyze design statistics, connectivity, and timing
- Run Design Rule Checks (DRCs)
- Run Weighted Average Simultaneous Switching Output (WASSO) analysis
- Partition and floorplan designs
- Queue multiple implementation attempts with various constraints
- Floorplan to improve performance
- Analyze implementation results to improve floorplanning
- Create and reuse module-level IP
- Update the top-level or module-level netlist

Course Outline

Day 1

- Course Overview
- **Lab 1:** Getting Started with PlanAhead
- Design Analysis and Exploration
- **Lab 2:** Design Analysis and Exploration
- Floorplanning Techniques
- **Lab 3:** Design Partitioning
- Creating a Top-level Floorplan
- **Lab 4:** Implementation
- Experimenting with Implementation Options

Day 2

- **Lab 5:** Floorplanning
- Creating a Floorplan for Performance
- **Lab 6:** Floorplan Tuning
- Tuning a Floorplan for Performance
- Block-Based Design and IP Reuse
- **Lab 7:** Block-Based Design and IP Reuse
- Netlist Updates and Incremental Design with PlanAhead
- **Lab 8:** Updating the Netlist
- Floorplanning Strategies
- Course Summary

Lab Descriptions

Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead software.

- **Lab 1:** Getting Started with PlanAhead – Illustrates the steps you take to import a synthesized design into the PlanAhead software so that you can begin floorplanning. Also introduces the PlanAhead environment and views.
- **Lab 2:** Design Analysis and Exploration – This lab introduces the analysis features of the PlanAhead software that enable early detection of potential design issues, alternate device selection, initial floorplanning direction, and post-implementation exploration.
- **Lab 3:** Design Partitioning – This lab introduces the concept of floorplanning. By using automated partitioning tools, you will create a top-level floorplan and experiment with sizing and shaping Pblocks based on resources assigned to them.
- **Lab 4:** Implementation – Introduces the integration of the ISE software implementation tools with the PlanAhead software. Also introduces a new tool called ExploreAhead to queue multiple ISE software runs with varying strategies.
- **Lab 5:** Floorplanning – Describes how to analyze implementation results and to use that information to generate a floorplan aimed at increasing design performance.
- **Lab 6:** Floorplan Tuning – Introduces techniques to help close on timing targets consistently.
- **Lab 7:** Block-Based Design and IP Reuse – Describes the steps to implement a block-based methodology that includes the creation and reuse of an IP module.
- **Lab 8:** Updating the Netlist – Illustrates the steps needed to update the project top-level netlist or at any module level.

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