

Course Description

Learn how to employ RocketIO™ MGT serial transceivers in your Virtex™-II Pro design. Understand and utilize the features of the RocketIO transceiver blocks, such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, synthesis and implementation considerations, and standards compliance. This course balances lecture modules and practical hands-on labs.

Level – Intermediate

Course Duration – 2 days

Price – \$1000 USD or 10 Training Credits

Course Part Number – RIO22000-8-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog or VHDL experience (or the *Introduction to Verilog* or the *Introduction to VHDL* course)
- Synthesis and simulation experience
- FPGA design experience or the *Fundamentals of FPGA Design* course
- Knowledge of high-speed serial I/O protocols and standards (SONET, Gigabit Ethernet, InfiniBand) is a plus

Software Tools

- ISE 8.1i
- ModelSim PE 6.0

After completing this comprehensive training, you will have the necessary skills to:

- Effectively use all of the advanced RocketIO features, such as CRC, channel bonding, clock correction, comma detection, 8b/10b encoding/decoding, programmable termination, and pre-emphasis
- Utilize the ports and attributes of RocketIO transceivers that control the RocketIO features
- Use the Architecture Wizard to instantiate RocketIO primitives in your design
- Achieve compatibility with high-speed I/O standards by using RocketIO transceivers

Course Outline

Day 1

- Introduction
- Clocking and Resets
- 8b/10b Encoder and Decoder Details
- **Lab 1:** 8b/10b Disparity and Bypass Lab
- Commas and Deserializer Alignment Details
- **Lab 2:** Commas and K-Characters Lab
- Cyclical Redundancy Check Details
- **Lab 3:** Cyclical Redundancy Check Lab
- Clock Correction Details
- **Lab 4:** Clock Correction Lab

Day 2

- Channel Bonding Details
- **Lab 5:** Channel Bonding Lab
- Architecture Wizard Overview
- Implementing a RocketIO Design
- **Lab 6:** Synthesis and Implementation Lab
- IP Overview: Aurora Reference Design
- **Lab 7:** Aurora Protocol Engine Lab
- Common Serial I/O Standards Compliance
- Physical Media Attachment Overview

Lab Descriptions

- **Lab 1:** 8b/10b Disparity and Bypass – Utilize the 8b/10b encoder/decoder and manipulate running disparity. Learn how to bypass the 8b/10b encoder/decoder
- **Lab 2:** Commas and K-Characters – Use programmable comma detection to align a serial data stream
- **Lab 3:** CRC – Modify a design to use the CRC feature for both the user mode and the Fiber Channel mode of CRC
- **Lab 4:** Clock Correction – Utilize the clock correction logic to compensate for frequency differences on the TX and RX side of a link
- **Lab 5:** Channel Bonding – Modify a design to use two transceivers bonded together to form one virtual channel
- **Lab 6:** Synthesis and Implementation – Use the Architecture Wizard to instantiate RocketIO primitives, synthesize a design, and implement the design.
- **Lab 7:** Aurora Protocol Engine – Use the Aurora reference design to send and receive data

Register Today

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