

Course Description

By learning PCI Express core protocol fundamentals, designers will gain a working knowledge of how PCI Express can be used in their systems. This course focuses on the PCI Express protocol subjects that designers, using the Xilinx PCI Express core, should understand to complete their designs faster and more easily. Students will also be introduced to each Xilinx PCI Express core product and will gain intimate knowledge of how the PCI Express core operates.

Level – Intermediate

Course Duration – 2 days

Price – \$1000 USD or 10 Training Credits

Course Part Number – PCIE28000-8-ILT

Who Should Attend? – Engineers who seek training in developing the necessary skills for designing PCI Express systems using Xilinx PCI Express cores

Prerequisites

- Basic PCI and/or PCI-X protocol knowledge
- Basic knowledge of Verilog or VHDL
- Basic experience with commonly used simulation tools like ModelSim
- Basic knowledge of Xilinx ISE™ software

Software Tools

- Xilinx ISE 8.1i
- Mentor Graphics ModelSim 6.0c PE

After completing this comprehensive training, you will have the necessary skills to:

- Effectively use the Xilinx PCI Express cores in your own design environments
- Select the appropriate PCI solution for a specific application
- Identify how PCI Express specification requirements apply to using Xilinx PCI Express cores

Course Outline

Day 1

- Overview
- Layers and Channels
- TLP Fields and Packet Routing
- PCI Express Local Link Interface
- **Lab 1:** Using the Local Link Interface
- PCI Express Configuration Space
- **Lab 2:** Exploring the Configuration Space

Day 2

- TLP Request and Completion Packets
- Generating Interrupts
- PCI Express Core Design Considerations
- **Lab 3:** Designing with the PCI Express Core
- PCI Express DMA Design Example
- **Lab 4:** PCI Express DMA Design Example
- Clocking and Other Physical Layer Topics
- Xilinx PCI Express Solutions
- **Lab 5:** Generating a Xilinx PCI Express Core

Lab Descriptions

- **Lab 1:** Using the Local Link Interface – Introduces the PCI Express core design that will also be used in Lab 2. It familiarizes you with the core user application interface (Local Link) and with modifying the design to change the packets being sent.
- **Lab 2:** Exploring the Configuration Space – Reinforces lessons learned in the previous modules by having you decode configuration packets to understand the requirements in configuring the core. In addition, you will see how to implement user configuration space.
- **Lab 3:** Designing with the PCI Express Core – Takes an in-depth look at designing with the core. You will become familiar with packet ordering and credits available.
- **Lab 4:** PCI Express DMA Design Example – Allows you to see how a simple, single-channel DMA example can be used with the PCI Express Core. You will also become familiar with allocating completion space for inbound completions.
- **Lab 5:** Generating a Xilinx PCI Express Core – Illustrates using the CORE Generator™ software to generate a core. The core is then implemented and you can verify the implementation by studying the various reports created by the Xilinx tools.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.