

Course Description

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

Level – Intermediate

Course Duration – 2 days

Price – \$1200 USD or 12 Training Credits

Course Part Number – DSP11000-82-ILT

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using The MathWorks MATLAB and Simulink and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with MATLAB and Simulink
- Basic understanding of sampling theory

Software Tools

- Xilinx ISE™ 8.2i SP1 with IP update 1
- Xilinx System Generator 8.2
- The MathWorks MATLAB with Simulink R14 SP3

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Recognize that hardware may be required for high-level abstraction
- Identify the high-level blocks available for FIR and FFT designs
- Perform hardware-in-the-loop and improve productivity
- Design a multiple clock-based System Generator system
- Employ various design techniques for improving system performance

Course Outline

Day 1

- Introduction to System Generator
- Simulink Basics
- **Lab 1:** Using Simulink
- Basic Xilinx Design Capture
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-based FIR Using the DSP48 Slice
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block

- Memories
- **Lab 7:** Designing with Shared Memories
- Achieving Higher Performance
- **Lab 8:** Improving Design Performance

Lab Descriptions

- **Lab 1:** Using Simulink – Learn how to use Simulink toolbox blocks and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Design a DSP48-based 12 x 8 MAC. Perform hardware-in-the-loop verification.
- **Lab 3:** Signal Routing – Design padding and unpadding logic using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR Using the DSP48 Slice – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware-in-the-loop.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity.
- **Lab 7:** Designing with Shared Memories – Learn to use multiple System Generator blocks to design and implement a multi-clock domain system.
- **Lab 8:** Improving Design Performance – Use the Timing Analyzer block and other techniques to improve system performance.

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