

### Course Description

This comprehensive course focuses on advanced simulation techniques that among other things, leverage the enhanced Verilog 2001 File IO capabilities. The course covers writing user-defined subprograms ( tasks and functions ) as part of creating a robust verification strategy.

The course also demonstrates important proprietary tool features and concepts, such as Code Coverage from MTI's ModelSim product, and Xilinx's own ISIM tool.

FPGA device level optimization is also discussed, from the standpoint of Verilog RTL coding, including using and simulating Xilinx CoreGen modules. In addition, back-annotated timing simulation techniques are demonstrated.

This course will enhance testing and verification skills for existing Verilog designers while improving quality-of-results for Xilinx FPGA based applications.

**Level** – Intermediate to Advanced

**Course Duration** – 2 days

**Price** – \$1000 USD or 10 Training Credits

**Practical HDL** Multimedia CD – \$195 USD

**Course Part Number** – LANG22000-8-ILT

**Who Should Attend?** – Engineers who want to use Advanced Verilog features for modeling and synthesis of digital designs

**Prerequisites**

- Basic digital design knowledge, Intro Verilog

**Software Tools**

- ISE™ 8.1i
- ModelSim 6.2 Simulator
- Synplicity Synplify Pro

At the end of this course, you'll be able to:

- Create tasks and functions for simulation
- Create self-checking test benches
- Use Verilog enhanced File IO capabilities
- Create basic scripts for automated Modelsim batch files
- Utilize important features of the ModelSim environment
- Discuss ModelSim support for System Verilog IEEE-1800
- Create an optimal Finite State Machine (FSM) using Verilog
- Target and optimize Xilinx FPGAs using Verilog
- Run a timing simulation using Xilinx Simprim libraries
- Create, Implement and simulate Xilinx CoreGen module
- Implement overall Verilog 2001 language enhancements

### Course Outline

#### Day 1

- Verilog tasks and functions
- ModelSim/ISIM Overview
- Advanced ModelSim/ISIM features
- **Lab 1: Create subprograms for simulation**
- Advanced Test bench Concepts
- Verilog 2001 Enhanced File I/O capability
- **Lab 2: Read input stimulus from external file**

#### Day 2

- Writing, storing and comparing outputs
- **Lab 3: Write simulation results to file**
- Strategies for self-checking test bench
- **Lab 4: Perform automated comparison, reporting**
- Using Xilinx CoreGen modules
- Advanced FPGA synthesis, timing constraints
- Code Coverage with ModelSim
- **Lab 5: Simulating with Code Coverage**

### Lab Description

The labs for this course offer a practical hands-on opportunity to create robust and re-usable testbenches. Each exercise is carefully constructed to permit discovery while exploring options and tradeoffs. In addition to the comprehensive step-by-step instructions, the lab documentation also provides additional insight regarding the tool, procedures or best-case practices.

### Register Today

Technically Speaking, Inc is the Xilinx ATP (Authorized Training Provider) for the North American Southwest region, including: southern California, Arizona, New Mexico and Nevada. TSI also delivers public and customized private courses in locations throughout the world.



To register for any course, or to discuss customized onsite training, contact TSI at **(702) 736-4116** or toll free at **(800) 706-4HDL**. Or register for public courses online at [www.technicallyspeaking.com/register.htm](http://www.technicallyspeaking.com/register.htm)

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

**Practical HDL** is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

**Cost** - \$195 USD

