Advanced VHDL

LANG21000-8-ILT (v1.0) **Course Specification**

Course Description

Increase your VHDL proficiency by learning advanced techniques that will help you write more robust and reusable code. This comprehensive course is targeted toward designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs as compared to lecture modules.

Level – Advanced
Course Duration – 2 days
Price – $1000 USD or 10 Training Credits
Course Part Number – LANG21000-8-ILT
Who Should Attend? – VHDL users with introductory to intermediate knowledge of VHDL
Prerequisites

- *Introduction to VHDL* course or equivalent knowledge of modeling, simulation, and RTL coding
- At least 6 months of coding experience beyond an introductory course

Software Tools

- Xilinx ISE™ 8.1i
- Mentor Graphics ModelSim PE 6.0c

After completing this comprehensive training, you will have the necessary skills to:

- Write efficient and reusable RTL, testbenches, and packages
- Create self-testing testbenches
- Create realistic models
- Use the Text IO capabilities of the VHDL language
- Store data dynamically
- Create parameterized designs

Course Outline

Day 1

- Course Introduction
- Modeling and Simulation I: Subprograms and Attributes
- Modeling and Simulation II: Access Types and Blocks
- **Lab 1:** Modeling
- Testbench Stimulus
- **Lab 2:** Model Testbench
- Utilizing Text IO
- **Lab 3:** Text IO Testbench

Day 2

- RTL Design and Xilinx
- Design Reuse and Parameterized Design
- **Lab 4:** RTL and Scalable Design
- Finite State Machines
- **Lab 5:** FSM and Scalable Design
- Simulation Issues Specific to Xilinx
- **Lab 6:** Xilinx and Scalable Design
- Course Review

Lab Descriptions

- **Lab 1:** Modeling – Write a hardware model utilizing generics, subprograms, generate statements, and access data types.
- **Lab 2:** Model Testbench – Write a self-testing testbench and simulate model.
- **Lab 3:** Text IO Testbench – Utilize VHDL Text IO operations in a self-testing testbench.
- **Lab 4:** RTL and Scalable Design – Write a reusable and scalable design block by utilizing synchronous design techniques.
- **Lab 5:** FSM and Scalable Design – Write a Finite State Machine (FSM) by utilizing FSM techniques for a high-performance FSM.
- **Lab 6:** Xilinx and Scalable Design – Optimize the design for Xilinx implementation. Simulate and implement the optimized design.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

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