

Course Description

This course introduces the new user to the Synplify Pro FPGA synthesis product. The course will familiarize the student with the FPGA design flow utilizing features of the Synplify Pro product, enabling the student to actively create designs using the Synplify Pro product.

Through the design experience of Synplicity® Corporate Application Engineers, students will learn to use the Synplify Pro product to design, debug, and implement FPGA and CPLD designs.

Level – Advanced

Course Duration – 1 day

Price – \$600 USD

Course Part Number – SYN-BAS-FPGA-101606

Who Should Attend? – FPGA Designers who are new to the Synplify Pro product.

Prerequisites

- Basic digital design knowledge, Verilog or VHDL
- HDL training is *NOT* part of this curriculum

Topics covered include:

- Project Management
- Synthesis Concepts
- The Interactive Text Editor with Error Cross-probing
- HDL Coding for performance
- SCOPE® Graphical Constraints Entry
- The Finite State Machine Tools
- Mapping to FPGA Technologies
- Debugging with the HDL Analyst® Option
- Timing Analyzer
- Batch Mode

Course Outline

Day 1

- Discussion of Need
- Introduction of Software Only Design
- **Lab 1: Building and Profiling S/W Only Solution**
- Design Review of Hardware Solution
- Connecting Hardware and Embedded System
- **Lab 2: Adding the Hardware Accelerator**
- Discussion of Other BRAM Uses
- Open Discussion and EDK Follow-up Summary

Register Today

TSI delivers public and private courses in locations throughout the world. Please contact us for more information, to view schedules, or to register online.

Visit www.technically-speaking.com for more company information,

Call **(702) 736-4116** for registration data or email us at eric@technically-speaking.com

Xilinx training credits cannot be honored at this time.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and training credits.

Practical HDL is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

Cost - \$195 USD

