

PCI-XP Glossary

Initialism	Meaning	Reference
ACK64	Acknowledge 64 bit mode.	This pin indicates that the card that is plugged into this slot is capable of 64 bit transfers.
AER	Advanced Error Reporting	
ANFE	Advisory Non-Fatal Error	
ASI	Advanced Switching Interconnect	
Asynchronous	Time independent	Time and bandwidth requirements vary per device
BAR	Base Address Register	Min size of decode space is 128 bytes
BCM	Byte Count Modified	For PCI-X only
C/BE	Byte Enable	Active low in header
CA	Completer Abort	Completion status code
CMM	Configuration Management Module	
Cold Reset	Fundamental reset at application of power	
Completer	Device that responds to the transaction	
CRS	Configuration Request Retry Status	Completion status code
D0-D3	Device power states – D0 is full power, D3-Cold is full off	
Data Credit	16 bytes	
Data Link Layer	Link management DLLPs	
Digest	Same as ECRC	
DLLP	Data Link Layer Packets	Manages single link, ack/nak, power management, flow control; always 8 bytes
ECRC	End-to-end CRC (must be enabled)	Always 32 bits long – EP bit and bit1 of format not included (header + data). Computed by core.
Egress Port	Output Port	
EMI	ElectroMagnetic Interference	
Endpoint	Requester or completer device at the end of a hierarchy domain	
EP	Error Parity – also known as "Poisoned" bit	TLP header – bit 14
ERR_COR	Error – Correctable	
Flow Control		Receiver periodically informs the transmitter of states of receive buffers. Replaces PCI retry/disconnect mechanisms
FSB	Front Side Bus (typically connects to memory)	
Header Credit	16 bytes for 4 DW header + 4 bytes for optional 1 DW ECRC	
Hierarchy	Set of all devices and links connected to all ports of the root complex	
Hierarchy domain	Set of all devices and links connected to one port of the root complex	
Hot reset	In-band mechanism propagates reset on link	
I/O Controller Hub	I/O Controller Hub	
Ingress Port	Input port	
IRDY		
isochronous	Time dependent	Time-sensitive transactions; must be guaranteed constant bandwidth
L0-L3	Link power states – L0 is full power, L3-Cold is full off	
Lane	Two links – one TX, the other RX for simultaneous serial data exchange	
Lane Reversal	Mismatch between order of Upstream and Downstream lane numbers	Some devices auto correct, Xilinx does not. PCI Express Specification section 4.2.5
LCRC	Layer CRC	Always 16 bits long
LTSSM	Link Training and Status State Machine	
M66En		
MCH	Memory Controller Hub	
MGT	Multi-Gigabit Transceiver	Hard-core on Xilinx FX families (and V2/Pro)
MPS	Maximum Payload Size	
MRL	Manually-operated Retention Latch	Used with Hot Swap capability
MSI	Message Signaled Interrupt	PCI Express Base Specification section 4.2.5. MSI-X covered in PCI v3.0 Specification 6.8.2
Non-Posted	Response required	
North Bridge	Connects processor to memory and graphics (typically) and to South Bridge	
Ordered Sets		Initialize link after power-on, reinitialize link during resume sequence, clock compensation
PCI-XP	Personal Computer Interface – Express	
PCIe	Same as PCI-XP	
PERR#	Parity Error	
PERST	Power Enable/Event Reset(?) - Fundamental Reset	
PMA	Physical Media Attachment	
PME	Power Management Event	
Port	Interface to the physical link	
Posted	No response required	
QoS	Quality of Service	
RCB	Read Completion Boundary	128 bytes for endpoints. Root is either 64 or 128 bytes
Requestor	Initiates a transaction	
Root Complex	Root of an I/O hierarchy that connects the CPU and memory to the I/O	Connects memory, CPU to the PCI-XP fabric; only device that generates configuration info
SC	Successful Completion	Completion status code
Sequence numbers		12-bit number applied by data link layer to TLPs. Allows transmitter to track success of packets
SERR#	System Error	When set, this enables both non-fatal and fatal errors to be reported to the Root Complex
SOF	Start of Frame	Indicates the beginning of the frame (active low)
SOP	Start of Payload	Indicates the beginning of the payload within the packet (active low)
South Bridge	Connects North Bridge to lower performance peripherals	
SSC	Spread-Spectrum Clocking	Used when dealing with PMA. defined by PCI Base Specification 4.3.3.1.1.1
STOP		
Switch	Device that is a virtual assembly of PCIe-to-PCIe bridges, allowing for multiple devices to exist within the PCIe hierarchy (type 1 configuration)	Will convert Type 1 to Type 0 and send to endpoints.
Synchronous/Non-Synchronous	Synchronous systems share the same clock, Non-Synchronous systems use different clocks	
Tags		TLPs are tagged with 8 bit value at the transaction layer. Associates with a completion packet for managing out-of-order (lower 5 bits used)
TC	Traffic Class	Xilinx Core only supports one TC; assigns priorities to certain types of packets; 8 values defined; Must map to a single VC. TC7 is highest priority.
TLP	Transaction Layer Packet	Communications transactions and events. r/w msg pkts, size varies depending on packet, pass through switches
Transaction Layer	"Topmost Layer" manages TX and RX. Assembles and disassembles TLPs	
TRDY		
Type 0	Targets endpoint – issued by root complex; device/vendor ID, BARs, PCI Express extended capabilities	
Type 1	Used to configure switches or bridges	Allows switches and PCI EX to be aware of address spaces used by downstream devices.
JR	Unsupported Request	Completion status code
VC	Virtual Channels	Xilinx Core only supports one VC; queues, buffers, control logic. 8 are defined
Warm Reset	Fundamental reset without re-application of power	