

Course Description

This comprehensive one day course offers a balance of language and tool specific topics that can greatly improve design verification results and enhance engineering productivity.

The fast-paced course covers how to fully leverage Verilog File I/O for both reading input stimulus from, and writing simulation results to external files. It also covers ModelSim specific features such as basic scripting, automated waveform comparison and Code coverage.

This class affords existing Verilog designers the opportunity to quickly apply advanced simulation techniques that immediately save time, promote consistency and yield an overall more robust design verification strategy.

Level – Intermediate to Advanced
Course Duration – 1 day
Price – \$600 USD
Practical HDL Multimedia CD – \$145 USD
Course Part Number – TSI-AMSVR-8-ILT
Who Should Attend? – Engineers who want to apply Advanced Verilog HDL simulation techniques within the ModelSim environment
Prerequisites

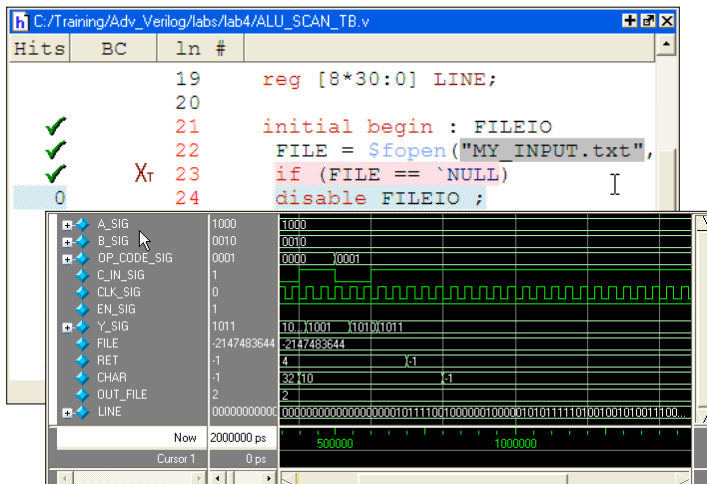
- Basic digital design knowledge, ModelSim, Intro Verilog

Software Tools

- ISE™ 8.2i
- ModelSim 6.2 Simulator
- Xilinx XST

At the end of this course, you'll be able to:

- Create tasks and functions for simulation
- Create self-checking test benches
- Use Verilog File I/O capabilities
- Read input stimulus from external files
- Write simulation results to external file
- Create basic scripts for automated Modelsim batch files
- Utilize ModelSim Automated waveform comparison
- Utilize ModelSim Code Coverage to evaluate test proficiency



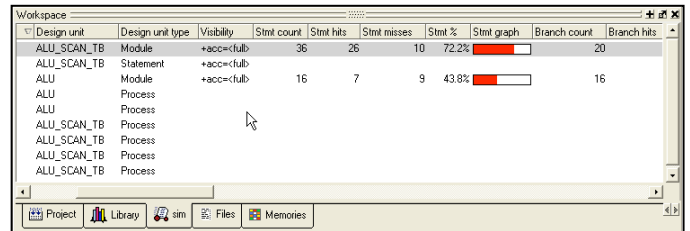
Course Outline

Day 1

- Advanced ModelSim Features
- Verilog tasks and functions and procedures
- Intro to Verilog File I/O
- Lab 1: Read input stimulus from external file**
- Advanced Verilog File I/O Concepts
- Lab 2: Compare simulation results, write to file**
- Using ModelSim Code Coverage Features
- Lab 3: Measure code coverage, improve scores**

Lab Description

The labs for this course offer a practical hands-on opportunity to create robust and re-usable verification strategies. Each exercise is carefully constructed to permit discovery while exploring options and tradeoffs. In addition to the comprehensive step-by-step instructions, the lab documentation also provides additional insight regarding the tools, procedures or best-case practices.



Register Today

Technically Speaking, Inc is the Xilinx ATP (Authorized Training Provider) for the North American Southwest region, including: southern California, Arizona, New Mexico and Nevada. TSI also delivers public and customized private courses in locations throughout the world.

To register for any course, or to discuss customized onsite training , contact TSI at (702) 736-4116 or toll free at (800) 706-4HDL. Alternately, you can register for public courses online at www.technically-speaking.com/register.htm

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

Practical HDL is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

Cost - \$145 USD

