

Course Description

Learn how to employ RocketIO™ GTP and GTX serial transceivers in your Spartan®-6 LXT or Virtex®-6 FPGA design. Understand and utilize the features of the RocketIO transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection. Additional topics include use of the Architecture Wizard, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

Level – Connectivity 3

Course Duration – 3 days

Price –

Course Part Number – RIO22000-12-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog or VHDL experience (or the *Introduction to Verilog* or the *Introduction to VHDL* course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of FPGA architecture and Xilinx implementation tools is helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Xilinx ISE® Design Suite: System Edition 12.1
- ChipScope™ Pro software 12.1
- Mentor Graphics ModelSim simulator 6.6a

Hardware

- Architecture: Spartan-6 and Virtex-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 board*

* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the ports and attributes of the RocketIO multi-gigabit transceiver in the Spartan-6 and Virtex-6 FPGA
- Effectively utilize the following features of the GTP/GTX:
 - 8B/10B and other encoding/decoding, comma detection, clock correction, and channel bonding
 - Pre-emphasis and linear equalization
- Use the GTP/GTX Wizard to instantiate GTP/GTX primitives in a design
- Access appropriate reference material for board design issues involving the power supply, reference clocking, and trace design

Course Outline

Day 1

- Spartan-6 and Virtex-6 Family Overview
- Transceiver Overview (GTP, GTX, GTH)
- Transceiver Clocking and Resets
- 8B/10B Encoder and Decoder
- **Lab 1:** 8B/10B Disparity and Bypass
- Commas and Deserializer Alignment
- **Lab 2:** Commas and Data Alignment

Day 2

- RX Elastic Buffer and Clock Correction

- **Lab 3:** Clock Correction
- Channel Bonding
- **Lab 4:** Channel Bonding
- Transceiver Wizard Overview
- **Lab 5:** GTP Wizard
- Implementing and Simulating a Transceiver Design
- **Lab 6:** Implementation and Simulation
- Physical Media Attachments

Day 3

- 64B/66B Encoding and the Gearbox
- **Lab 7:** 64B/66B GTX Transceiver
- Transceiver-Specific Board Design Considerations
- RocketIO Transceiver Test and Debugging
- **Lab 8:** System Lab
- RocketIO Transceiver Application Examples

Lab Descriptions

- **Lab 1:** 8B/10B Disparity and Bypass – Utilize the 8B/10B encoder and decoder and observe running disparity. Learn how to bypass the 8B/10B encoder and decoder.
- **Lab 2:** Commas and Data Alignment – Use programmable comma detection to align a serial data stream.
- **Lab 3:** Clock Correction – Utilize the attributes and ports associated with clock correction to compensate for frequency differences in the TX and RX clocks.
- **Lab 4:** Channel Bonding – Modify a design to use two transceivers bonded together to form one virtual channel.
- **Lab 5:** GTP Wizard – Use the GTP Wizard to create instantiation templates
- **Lab 6:** Implementation and Simulation – Instantiate the transceiver component in a design, synthesize the design, and implement the design.
- **Lab 7:** 64B/66B GTX Transceiver – Generate a 64B/66B GTX core by using the CORE Generator™ tool, simulate the design, and analyze the results.
- **Lab 8:** System – Perform all design steps from planning the design, generation of the core, integration of the core into a design, simulating, implementing and debugging the design, and optimizing the link parameter using an evaluation board.

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