Adv Xilinx Timing Closure

w/ Synplify Pro®, XST® & PlanAhead®

TSI_11230-12-ILT (v1.0) **Course Specification**

Course Description

This custom hybrid course is a fast-paced --lab intensive curriculum that focuses on Xilinx chip-level optimization when using Synplify Pro® or Xilinx XST® for design entry. The course covers specific synthesis options that can enhance performance and results. It then covers comprehensive Xilinx timing constraints that are critical to driving the P&R tools. The course ends with using the PlanAhead® tool to manage layout, improve timing and enhance repeatability. This course can help you fit your design into a smaller FPGA or a lower speed grade for reducing system costs. In addition, by mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten development time & lower development costs.

Level – FPGA 3
Course Duration – 2 days
Price – $1400 USD or 14 Xilinx TCs

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and some experience with the Xilinx ISE® software tools

Prerequisites

- *Essentials of FPGA Design* course or equivalent knowledge of FPGA architecture features; the Xilinx implementation software flow and implementation options; reading timing reports; basic FPGA design techniques; global timing constraints and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Recommended RELs

- Basic HDL Coding Techniques REL (parts 1 and 2)
- Virtex-6 & Spartan-6 FPGA HDL Coding Techniques REL (parts 1 and 2)
- Power Estimation REL

Software Tools

- ISE Design Suite: Logic or System Edition 12.1
  PlanAhead 12.1 & Synplify Pro

Hardware

- Architecture: Spartan®-6 and Virtex-6 FPGAs*

* This course focuses on the Spartan-6 and Virtex-6 architectures. .

After completing this comprehensive training, you will have the necessary skills to:

- Use key Synplify/Pro features to enhance QoR
- Use key Xilinx XST features to enhance QoR
- Describe a flow for obtaining timing closure
- Describe architectural features of the Xilinx FPGAs
- Describe the features of the Digital Clock Manager (DCM) and Phase-Locked Loop (PLL), Multi-Mode Clock Manager (MMCM) and how they can be used to improve performance
- Pinpoint design bottlenecks by using the Timing Analyzer
- Apply advanced timing constraints to meet timing
- Use PlanAhead to evaluate and optimize logic placement

Course Outline

Day 1

- Course Introduction
- Xilinx Timing Closure Design Overview
- Synthesis Optimization with Synplify Pro
- Synthesis Optimization with XST
- **Lab 1:** Use Advance Synthesis Options
- Xilinx FPGA Clocking Resources, V6, Spartan-6
- **Lab 2:** Create various clocking schemes
- Comprehensive Timing Constraints
- **Lab 3:** Create Detailed Timing Groups

Day 2

Using Xilinx Timing Analyzer

- Xilinx PlanAhead (Part I)
- **Lab 4:** Getting started with PlanAhead
- Xilinx PlanAhead (Part II)
- **Lab 5:** Creating Floorplans, Analyzing Results
- Xilinx PlanAhead (Part III)
- **Lab 6:** Fine-tuning Floorplans
- Course Review

Lab Descriptions

Lab 1: Advanced Synthesis Options - For either VHDL or Verilog users, understanding key synthesis options and menu selections

- **Lab 2:** Create Various Clocking schemes - Use the Architectural Wizard to create DCM or MMCM components for various clock frequencies and distribution requirements
- **Lab 3:** Create Detailed Timing Groups - Use the Xilinx Constraints Editor to create comprehensive Timing Constraints
- **Lab 4:** Getting Started with PlanAhead - Create projects, perform initial design analysis
- **Lab 5:** Creating Floorplans, Analyzing Results - Create floorplan, implement design, evaluate results
- **Lab 6:** Export IP Module - Create RPMs for module reuse, portability and deterministic layout

Register Today

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