DSP Design Using System Generator

DSP 3

DSP11000-11-ILT (v1.0)

Course Specification

Course Description

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Level – DSP 3
Course Duration – 2 days
Price –
Course Part Number – DSP11000-11-ILT
Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools

- Xilinx ISE® Design Suite: System Edition 11.3
- MATLAB with Simulink software R2008b or R2009a

Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 board*

* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Identify the high-level blocks available for FIR and FFT designs
- Design a multiple-clock-based System Generator system
- Embed two System Generator designs into a larger design
- Use a custom-designed FPGA PCB as a hardware co-simulation target

Course Outline

Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- Xilinx System Generator, Project Navigator, and Platform Studio Integration
- **Lab 7:** System Generator and Project Navigator Integration

Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 7:** System Generator and Project Navigator Integration – Learn how to embed two System Generator designs into a larger design and how VHDL created by System Generator can be incorporated into the simulation model of the overall system.

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