

Course Description

This fully –loaded, fast paced one day course offers a balance of language and tool specific topics that can greatly improve design verification results and enhance engineering productivity.

We'll cover how to fully leverage VHDL Text I/O for both reading input stimulus from, and writing simulation results to external files. We also cover Mentor Graphic's ModelSim specific features such as basic scripting, automated waveform comparison and Code coverage.

For Xilinx ISE users, the class also covers how to leverage the interface between the Xilinx tools and ModelSim for maximum productivity.

This class affords existing VHDL designers the opportunity to quickly apply advanced simulation techniques that immediately save time, promote consistency and yield an overall more robust design verification strategy.

Level – Intermediate to Advanced
Course Duration – 1 day
Price – \$600 USD or 6 Xilinx TCs
Practical HDL Multimedia CD – \$145 USD
Course Part Number – TSI-AMSVHD-11-ILT
Who Should Attend? – Engineers who want to apply Advanced VHDL simulation techniques within both the ISE & ModelSim environment, including simulating IP cores
Prerequisites

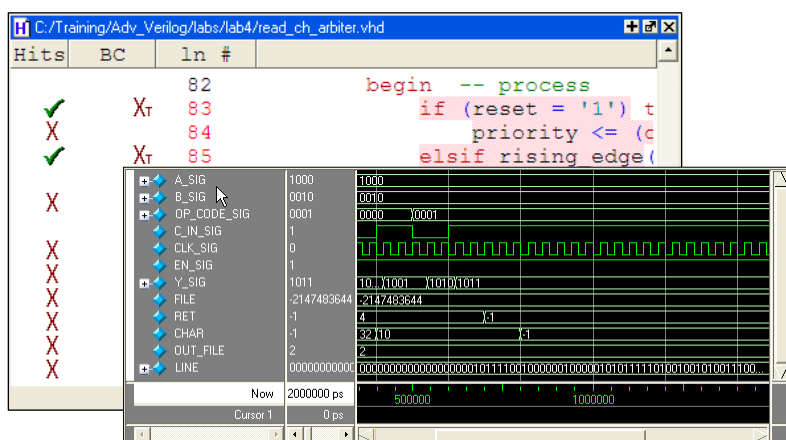
- Basic digital design knowledge, ModelSim, Intro VHDL

Software Tools

- ISE™ 11.1i
- ModelSim 6.4 Simulator

At the end of this course, you'll be able to:

- Create procedures and functions for simulation
- Create self-checking test benches
- Use VHDL Text I/O capabilities
- Read input stimulus from external files
- Write simulation results to external file
- Create basic scripts for automated Modelsim batch files
- Utilize ModelSim Automated waveform comparison
- Utilize ModelSim Code Coverage to evaluate test proficiency



Course Outline

Day 1

- Advanced Simulation Techniques
- Simulating IP Cores
- Lab 1: Simulating IP Cores**
- Advanced ModelSim Features
- Intro to VHDL Text I/O
- Lab 2: Read input stimulus from external file**
- Advanced VHDL Text I/O Concepts
- Lab 3: Compare simulation results, write to file**
- Using ModelSim Code Coverage Features
- Lab 4: Measure code coverage, improve metrics**

Lab Description

The labs for this course offer a practical hands-on opportunity to create robust and re-usable verification strategies. Each exercise is carefully constructed to permit discovery while exploring options and tradeoffs. In addition to the comprehensive step-by-step instructions, the lab documentation also provides additional insight regarding the tools, procedures or best-case practices.

Register Today

Technically Speaking, Inc is the Xilinx ATP (Authorized Training Provider) for the North American Southwest region, including: southern California, Arizona, New Mexico and Nevada. TSI also delivers public and customized private courses in locations throughout the world.

To register for any course, or to discuss customized onsite training , contact TSI at (702) 736-4116 or toll free at (877) TSI-1HDL. Alternately, you can register for public courses online at www.technically-speaking.com/register.htm

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, Discover, or American Express) as well as purchase orders and Xilinx training credits.

Practical HDL is a comprehensive VHDL/Verilog self-paced multimedia training environment.

This tool both reinforces topics covered during the class and offers additional advanced subject matter.

Cost - \$145 USD

